11. (Amended) A method for fabricating a semiconductor device according to claim 6, wherein the heavy ions are implanted at such an implant energy as getting a range of the heavy ions located inside the extended high-concentration dopant diffused layer.

12. (Amended) A method for fabricating a semiconductor device according to claim 6, wherein the heavy ions are implanted at such an implant energy as making a range of the heavy ions equal to or deeper than a range of the first dopant and between one to three times as deep as the range of the first dopant.

14. (Amended) A method for fabricating a semiconductor device according to claim 13, wherein an implant dose of the indium ions is $5 \times 10^{13}/cm^2$ or more.

REMARKS

At the outset the Examiner is thanked for the review and consideration of the present application.

The Examiner's Office Action dated February 11, 2002 has been received and its contents reviewed. Claims 1-19 were pending in the present application. Claims 1-5, 16 and 17 have been withdrawn from further consideration. By this Amendment, claims 6, 8, 9, 11, 12 and 14 have been amended, and claims 16-19 have been canceled. Accordingly, claims 1-15 are pending, of which claims 1 and 6 are independent.

Turning to the detailed Office Action, claim 8 is objected as containing informalities, and claim 19 is objected to under 37 C.F.R. 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. In response, Applicants have amended claim 8 to replace "sidewall" with "sidewall spacer" to correct the informalities.

With respect to claim 19, the objection to claim 19 is now rendered moot by its cancellation.

Claims 9, 11, and 12 are rejected under 35 U.S.C. §112, second paragraph, as indefinite and failing to conform with current U.S. practice. Claim 9 improper recites implantation of ions, at a level equal to or deeper than a range of the first dopant and shallower than a range of the first dopant. In response, Applicants have amended claim 9 to recite "shallower than a range of the second dopant."

Claim 11 recites a feature wherein the heavy ions are implanted at an energy level making a range of the first dopant (15) located inside the extended high-concentration dopant diffused layer (15), while claim 6 recites that the first dopant forms the extended high-concentration dopant diffused layer. As such, a layer cannot be inside or shallower than itself. In response, Applicants have amended claim 11 to replace "first dopant" with "heavy ions", as shown above, to correctly recite the present invention.

Claim 12 incorrectly recites that the depth of the implanted heavy ions be both equal to or deeper than and shallower (three times or less) than a range of the first dopant at the same time. In response, Applicants have amended claim 12, as shown above, to provide a clearer claim language.

Claim 14 has no proper antecedent basis for the feature "indium ions". In response, Applicants have amended claim 14 to change its dependency to claim 13 where proper antecedent basis is found.

With respect to claims 9, 11, and 12, the Examiner asserts that the phrase "such...as" in line 3 renders the claim indefinite. In response, Applicants respectfully submit that, according to MPEP 2173.05(d), the exemplary language "for example" and "such as" could render a claim indefinite. However, in claims 9, 11, and 12, the language "such ... as" particularly used in the phrase "at such an implant energy as forming...", in claim 9, for example, is **NOT** an exemplary language specified by MPEP 2173.05(d). In other words, "such as" does not have the same meaning as "such...as" found in claims 9, 11, and 12. Therefore, the basis for this rejection is incorrect. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 9, 11, and 12 based on MPEP 2173.05(d).

Claims 6, 7, 11, and 12 are rejected under 35 U.S.C. 102(b) as clearly anticipated by Kita (JP 06-267974). Further, claims 8, 9, 13, 14, 18, and 19 are rejected under 35 U.S.C. 103(a) as unpatentable over Kita and further in view of Sultan (U.S. Patent No. 5,970,353), and claim 10 rejected under 35 U.S.C. 103(a) as unpatentable over Kita and further in view of Anjum et al. (U.S. Patent No. 6,331,458 - hereafter Anjum). The rejections are respectfully traversed at least for the reasons provided below.

As amended, claim 6 recites the steps of implanting heavy ions into a semiconductor region, thereby forming a first ion implanted layer of a second conductivity, at least upper part of which is an amorphous layer; implanting ions of a first dopant into the semiconductor region, in

which the amorphous layer has been formed, thereby forming a second ion implanted layer of the first conductivity type; and conducting a first annealing process, thereby forming an extended high-concentration dopant diffused layer of the first conductivity type through diffusion of the first dopant and a pocket dopant diffused layer of the second conductivity type, which is located under the extended high-concentration dopant diffused layer, through diffusion of the heavy ions, respectively, wherein the pocket dopant diffused layer includes a segregated part that has been formed through segregation of the heavy ions.

According to the amended claim 6, heavy ions are used to form the pocket dopant diffused layer of the second conductivity type. Thus, pre-amorphization effects are attainable by the implantation of the heavy ions, and a dislocation loop layer can advantageously trap the silicon interstitials. In addition, since the heavy ions are easily trapped and segregated in the dislocation loop layer, the extended high-concentration dopant diffused layer and pocket dopant diffused layer can both have their junctions shallowed and sharpened, as . Accordingly, a miniaturized semiconductor device and a fabrication process thereof can be provided with the inverse channel effects suppressed.

Turning to the cited reference, Kita teaches the step of : ion implanting silicon (6) to convert a silicon semiconductor substrate (1) to an amorphous state, forming a p-type diffusion layer 5 by ion implanting boron (7) into the main surface of the semiconductor substrate, and annealing to re-crystallize the semiconductor substrate in the amorphous state. Kita also teaches that non-active elements such as argon, krypton and the like can be used for ion implantation of the semiconductor substrate in the amorphous state.

As noted above, according to the amended claim 6 of the present invention, the extended high-concentration dopant diffused layer and pocket dopant diffused layer can both have their junctions shallowed and sharpened by using heavy ions to form the pocket dopant diffused layer of the second conductivity type.

—> On the other hand, Kita only teaches ion implanting silicon, argon, krypton and the like to convert a silicon semiconductor substrate (1) to an amorphous state. Further, Kita completely fails to disclose the step of forming the amorphous layer by implanting heavy ions and the step of forming the pocket dopant diffused layer of the second conductivity type as recited in amended claim 6.

Moreover, as shown in Fig. 1D of Kita, since the p-type diffusion layer 5 is formed after annealing, it is clear that the pocket dopant diffused layer is not formed.

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. Lindemann Maschinenfabirk Gmbh v. American Hoist & Derrick, 221 USPQ 481, 485 (Fed. Cir. 1984). Kita clearly fails to disclose the method positively recited and claimed in applicants independent claim 6. More particularly, Kita fails to disclose a second step of implanting heavy ions into a semiconductor region using the gate electrode as a mask, thereby forming a first ion implanted layer of the second conductivity, at least upper part of which is an amorphous layer, and hence forming a pocket dopant diffused layer of the second conductivity type. Therefore, the application of Kita in the §102(e) rejection is improper.

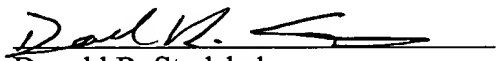
With respect to the §103(a) rejection of claims 8, 9, 10, 13, 14, 18, and 19, the arguments set forth above in relation to the rejection of independent claim 6 also are applicable to the §103(a) rejection of claims 8, 9, 10, 13, and 14. Further, the cancellation of claims 16-19 renders their rejection moot.

Accordingly, Applicants respectfully request reconsideration and withdrawal of the §102(e) rejection of claim 6 and its dependent claims, as well as the §103(a) rejection of claims 8, 9, 10, 13, 14, 18, and 19.

CONCLUSION

Having responded to the rejection set forth in the outstanding non-Final Office Action, it is submitted that claims 6-15 are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,



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MARKED-UP VERSION OF AMENDED CLAIMS:

6. (Amended) A method for fabricating a semiconductor device that includes an extended high-concentration dopant diffused layer of a first conductivity and a pocket dopant diffused layer of a second conductivity, comprising:

a first step of forming a gate electrode over a semiconductor region with a gate insulating film interposed therebetween;

a second step of implanting heavy ions into the semiconductor region using the gate electrode as a mask, thereby forming a first ion implanted layer of the second conductivity, at least upper part of which is an amorphous layer;

a third step of implanting ions of a first dopant into the semiconductor region, in which the amorphous layer has been formed, using the gate electrode as a mask, thereby forming a second ion implanted layer of [a] the first conductivity type; and

a fourth step of conducting a first annealing process to activate the first and second ion implanted layers, thereby forming [an] the extended high-concentration dopant diffused layer of the first conductivity type through diffusion of the first dopant and [a] the pocket dopant diffused layer of the second conductivity type, which is located under the extended high-concentration dopant diffused layer, through diffusion of the heavy ions, respectively,

wherein the pocket dopant diffused layer includes a segregated part that has been formed through segregation of the heavy ions.

8. (Amended) A method for fabricating a semiconductor device according to claim 6, further comprising the steps of:

forming a sidewall spacer on side faces of the gate electrode after the third step has been performed;

implanting ions of a [third] second dopant into the semiconductor region using the gate electrode and the sidewall spacer as a mask, thereby forming a third ion implanted layer of the first conductivity type; and

conducting a second annealing process to activate the third ion implanted layer, thereby forming a high-concentration dopant diffused layer of the first conductivity type, which is located outside of the extended high-concentration dopant diffused layer, has a junction deeper

than that of the extended high-concentration dopant diffused layer and has been formed through diffusion of a second dopant.

9. (Amended) A method for fabricating a semiconductor device according to claim 8, wherein the heavy ions are implanted at such an implant energy as forming an amorphous/crystalline interface, through implantation of the heavy ions, at a level equal to or deeper than a range of the first dopant and shallower than a range of the [first] second dopant.

11. (Amended) A method for fabricating a semiconductor device according to claim 6, wherein the heavy ions are implanted at such an implant energy as getting a range of the [first dopant] heavy ions located inside the extended high-concentration dopant diffused layer.

12. (Amended) A method for fabricating a semiconductor device according to claim 6, wherein the heavy ions are implanted at such an implant energy as making a range of the heavy ions equal to or deeper than a range of the first dopant and between one to three times [or less] as deep as the range of the first dopant.

14. (Amended) A method for fabricating a semiconductor device according to claim [6] 13, wherein an implant dose of the indium ions is $5 \times 10^{13}/cm^2$ or more.